**Listing of Claims:**

1. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate with a patterned and etched layer of gate oxide over the surface thereof and a patterned and etched layer of gate material over said patterned gate oxide, a LDD impurity implant into the substrate having been performed and annealed self-aligned with the patterned and etched layer of gate material;

performing a plasma treatment directly on the patterned and etched layer of gate material and directly on exposed surfaces of the provided substrate, ~~wherein there are no layers separating the exposed surfaces of the provided substrate from the plasma treatment~~ wherein a gas based layer is formed over the patterned and etched layer of gate material and the exposed surfaces of the provided substrate after performing the plasma treatment; and

creating spacers over sidewalls of the patterned and etched layer of gate material.

2. (Previously Presented) The method of claim 1, the plasma exposure being a H2 based plasma exposure.

3. (Previously Presented) The method of claim 1, the plasma exposure being an O2 based plasma exposure.

4. (Original) The method of claim 1, the plasma exposure being a N2 based plasma exposure.

5. (Original) The method of claim 1, additionally pocket implants having been performed into the substrate after the LDD impurity implant have been performed.

6. (Original) The method of claim 1, additionally completing the gate electrode and conductive interconnects there-to after creating spacers over sidewalls of the patterned and etched layer of gate material.

7. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing an impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing a plasma treatment directly on the sidewalls of the gate electrode and directly on the exposed substrate, wherein a gas based layer is formed over the sidewalls of the gate electrode and the exposed substrate after performing the plasma treatment;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

8. (Original) The method of claim 7, the plasma treatment being a H2 based plasma exposure.

9. (Previously Presented) The method of claim 7, the plasma treatment being an O2 based plasma exposure.

10. (Original) The method of claim 7, the plasma treatment being a N2 based plasma exposure.

11. (Original) The method of claim 7, the impurity implant comprising LDD implants.

12. (Original) The method of claim 7, the impurity implant comprising LDD implants followed by pocket implants.

13. (Original) The method of claim 7, the impurity implant being followed by an anneal.

14. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide; creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing a H2 based plasma treatment directly on the sidewalls of the gate electrode and directly on the exposed substrate, wherein a hydrogen based layer is formed over the sidewalls of the gate electrode and the exposed substrate after performing the H2 based plasma treatment;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

15. (Original) The method of claim 14, the impurity implants comprising LDD implants.

16. (Original) The method of claim 14, the impurity implants comprising LDD implants followed by pocket implants.

17. (Original) The method of claim 14, the impurity implants being followed by an anneal.

18. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing an [[02]] O2 based plasma treatment directly on the sidewalls of the gate electrode and directly on the exposed substrate, wherein an oxide based layer is formed over the sidewalls of the gate electrode and the exposed substrate after performing the O2 based plasma treatment;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

19. (Original) The method of claim 18, the impurity implants comprising LDD implants.

20. (Original) The method of claim 18, the impurity implants comprising LDD implants followed by pocket implants.

21. (Original) The method of claim 18, the impurity implants being followed by an anneal.

22. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing a N2 based plasma treatment directly on the sidewalls of the gate electrode and directly on the exposed substrate, wherein a nitrogen based layer is formed over the sidewalls of the gate electrode and the exposed substrate after performing the N2 based plasma treatment;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

23. (Original) The method of claim 22, the impurity implants comprising LDD implants.

24. (Original) The method of claim 22, the impurity implants comprising LDD implants followed by pocket implants.

25. (Original) The method of claim 22, the impurity implants being followed by an anneal.

26. (Currently Amended) A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing a LDD impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing a pocket impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing an anneal of the LDD and pocket impurity implants;

performing a H2 based or an N2 based or an O2 based plasma treatment directly on the sidewalls of the gate electrode and directly on the exposed substrate, wherein a H2 based or an N2 based or an O2 based layer is formed over the sidewalls of the gate electrode and the exposed substrate after performing the H2 based or the N2 based or the O2 based plasma treatment;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

27. (Currently Amended) A method of manufacturing a gate electrode, comprising:

providing a substrate;

forming a patterned gate oxide over said substrate;

forming a patterned gate material over said patterned gate oxide;

forming a pair of LDD structures in said substrate and respectively adjacent to said patterned gate oxide;

performing a plasma treatment directly to said patterned gate material and directly to said substrate, wherein a gas based layer is formed over the patterned gate material and the substrate after performing the plasma treatment; and

respectively forming a pair of spacers over sidewalls of said patterned gate oxide and gate material following the plasma treatment.

28. (Original) The method of claim 27, the plasma treatment being a H2 based plasma treatment.

29. (Previously presented) The method of claim 27, the plasma treatment being an O2 based plasma treatment.

30. (Original) The method of claim 27, the plasma treatment being a N2 based plasma treatment.

31. (Original) The method of claim 27, the forming a pair of LDD structures being followed by an anneal.

32. (Currently Amended) A method of manufacturing a gate electrode, comprising the sequential steps of:

providing a substrate;

forming a patterned gate oxide over said substrate;

forming a patterned gate material over said patterned gate oxide;

forming a pair of LDD structures in said substrate and respectively adjacent to said patterned gate oxide;

performing a plasma treatment directly to said patterned gate material and directly to said substrate, wherein a gas based layer is formed over the patterned gate material and the substrate after performing the plasma treatment; and

respectively forming a pair of spacers over sidewalls of said patterned gate oxide and gate material.